Race Around Condition

STUDYBYNOTES

- The race around condition for J-K Flip-flop, if J=K=1 and if clk = 1 for a long period of time, the Q output will ~~toggle~~ toggle as long as clk high which makes the output of the flip flop unstable or uncertain.
  This problem is called race around condition in J-K Flip flop.

- Race Around Condition can be avoided by ensuring that the clock input is at logic "1" only for a very short time.

- This Introduced the concept of Master Slave JK flip flop.

C	J	K
1	1	1

↳ toggling place occur.

Methods to Remove Race Around Condition

Race condition can be removed in the following ways:-

(i) Increasing the delay of flip-flop

→ The Propagation delay should be made greater than the duration of clock pulse (T).

i.e. $T/2 <$ Propagation delay of flip flop.

(But it is not good solution as increasing the delay will decrease the speed of the system.

(ii) Use of edge-bigged flip flop

(iii) Use of Master-Slave JK flip flop

→ The race around condition can be removed with Master Slave JK flip flop.

Master-Slave JK Flip Flop

STUDYBYNOTES

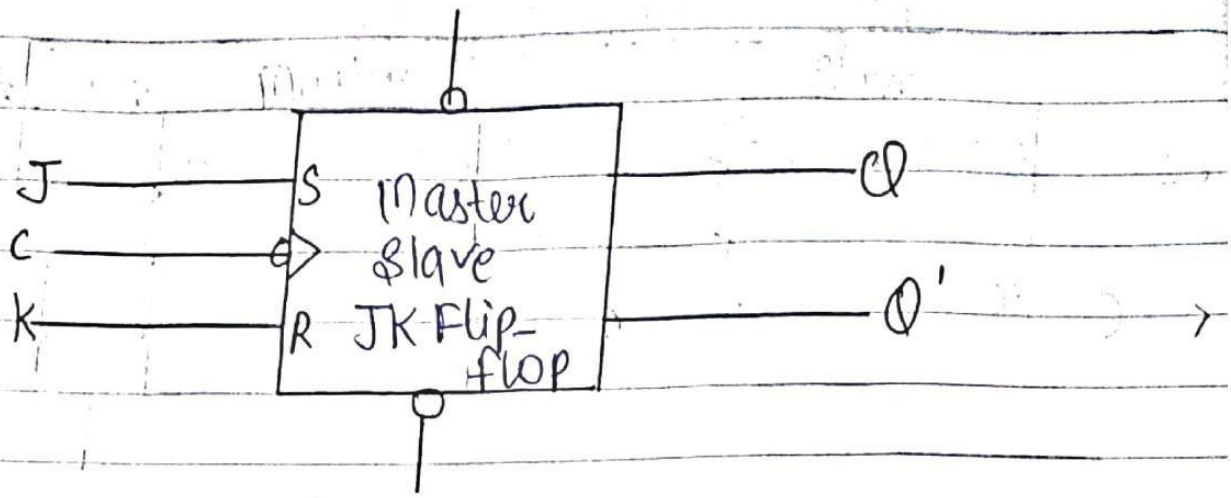
- The master-slave flip flop is constructed by combining two JK Flip Flop. These flip flops are connected in a series configuration.

- In these two flip flops, the 1st flip flop work as "master" called the master flip-flop.
  and the 2nd work as a "slave" called slave flip flop.

- The output from the master flip-flop is connected to the two inputs of the slave flip flop whose output is fed back to inputs of the master flip.

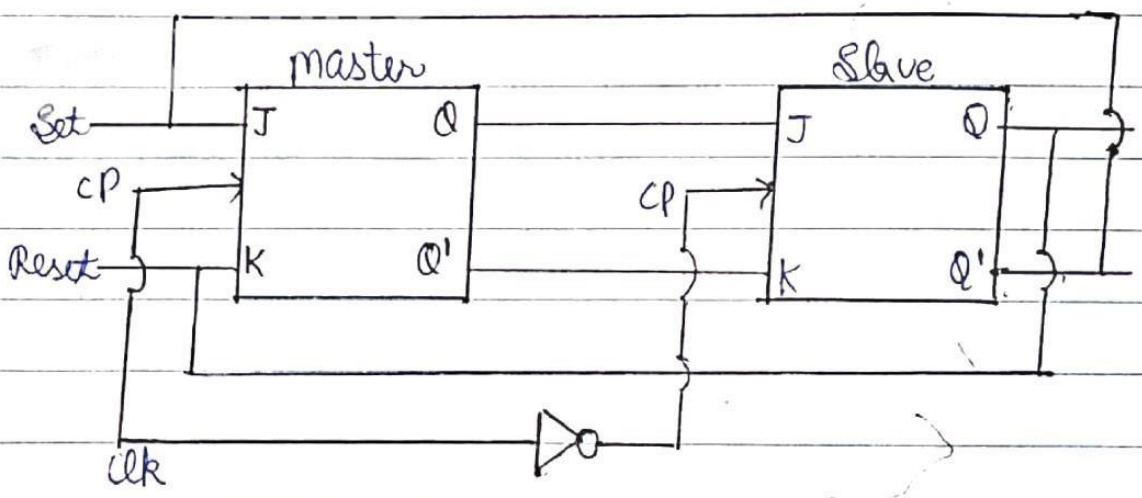
- and one circuit also includes as an inverter.

- In other words, If C=0 for a master flip flop, the C=1 for a slave ff. and if C=1 for master ff, then becomes 0 for



Block Diagram of :-
Master Slave JK flip flop

Logic Diagram



Master Slave JK flip flop

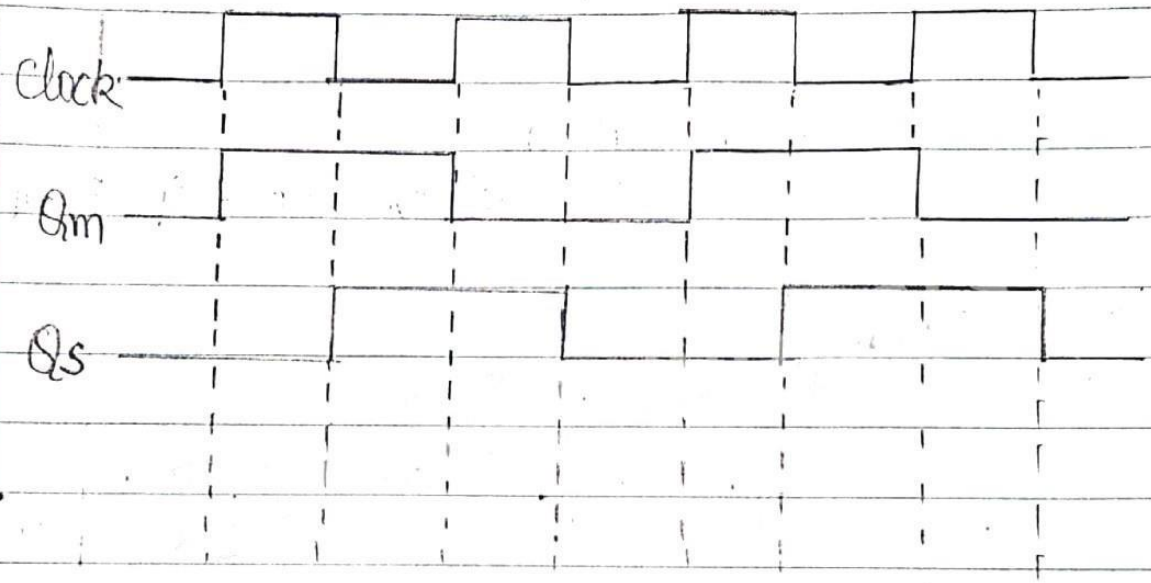
When clock is Low :-

- When the clock pulse (C) is 0, then slave Flip-Fip is enabled and master flip-flop is disabled.

The O/p of slave follows the O/p of master f/f, but during this time master f/f does not respond.

When Clock is High:-
When the master is enabled and it follows the truth table of JK flip flop, but Slave not respond.

Timing Diagram of a Master flip-flop



- When the clock pulse set to 1. the, the output of the master flip flop will be one until the clock input remains 0.
- The master flip flop is operational when the clock pulse is 1.
- The Slave flip flop is operational when the clock pulse is 0.

⊛ Applications of Flip-flops

- There are the various types of flip-flops being used in digital electronic circuits.
- The applications of flip-flops are as specified below :-

1. Latch
2. Counters
3. Data transfer
4. Data Storage
5. Registers
6. Memory
7. Shift-Registers
8. Storage-Registers
9. Sequence Generator.
10. Resistors.