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An electronic circuit in which the output depends upon the present combination of the input.

Or

Combinational circuits – Combination of 2 or more logic gates is called combinational circuits.

6 types

1. Half adder
2. Full adder
3. Decoder
4. Encoder
5. Multiplexer
6. De multiplexer

---

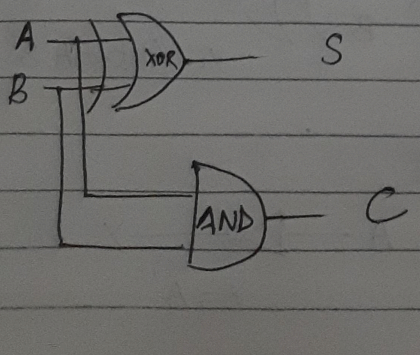
① **Half Adder** – It is used to add 2 bits/digits. It has 2 inputs and 2 outputs.
The first output is for sum (S)
The second output is for carry (C).

Q How 2 bits are added?

```
   0        0        1        1
 + 0      + 1      + 0      + 1
 ----     ----     ----     ----
 0  0     0  1     0  1     1  0
 C  S     C  S     C  S     C  S.
```

All four operations are done by the half adder (H.A)
It is made up of 2 logic gates

① XOR Gate ② AND Gate.



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The working of half adder can be explained with the help of a truth table.

A	B	S (XOR)	C (AND)
0	0	0	0
0	1	1	0
1	0	1	0
Φ	1	0	1

Logic eqⁿ for half adder.

$$Sum = A \oplus B = A'.B + A.B'$$

$$Carry = A \cdot B$$

② Full adder - It is used to add 2 binary numbers. It has 3 inputs and 2 outputs. The 3rd input is for carry generated by the previous digits.

It is made up of
↓ ↓ ↓
① XOR gate ② AND gate ③ OR gate.

Here, $S = A \oplus B \oplus C$

$$C = AB + BC + AC$$

$$C = (A \oplus B).C + A.B$$

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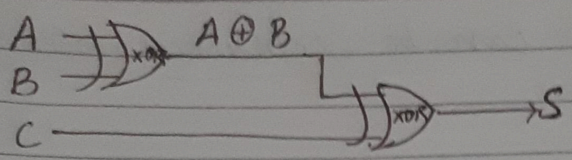

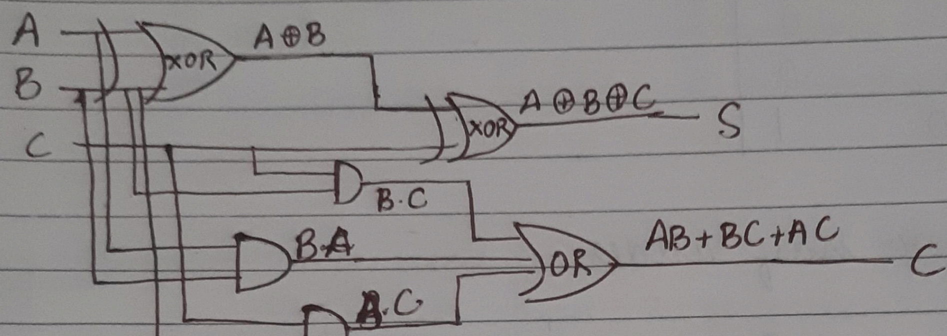

The working of full adder can be explained using its truth table :

A	B	C	S	C
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

<u>Parallel Adder</u> – It is a combination of various full adders.

for ex. 4 bit parallel adder has 4 full adders.

A_1 A_2 A_3 A_4
1 1 0 1
B_1 1 B_2 1 B_3 1 B_4 0
11 0 1 1

X

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(3) <u>Decoder</u> - It is a combinational circuit that converts binary digits into equivalent decimal numbers.

In other words it converts 'n' binary digits into equivalent decimal codes.

It may have <u>n inputs</u> and <u>2^n outputs</u>.

ex: let us have n=3 inputs, then we have $2^n = 8$ outputs

Such a decoder is known as <u>3 to 8 line decoder</u>

ie: <u>n to 2^n line decoder</u>

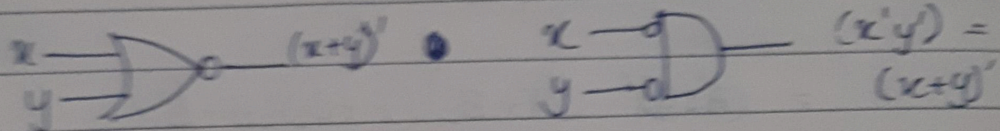
I_1	I_2	I_3	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	1	0	0	0	0	0	0	1	0	0
0	1	1	0	0	0	0	1	0	0	0
1	0	0	0	0	0	1	0	0	0	0
1	0	1	0	0	1	0	0	0	0	0
1	1	0	0	1	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0

De-Morgan's Theorem - used while dealing with NOR and NAND gates

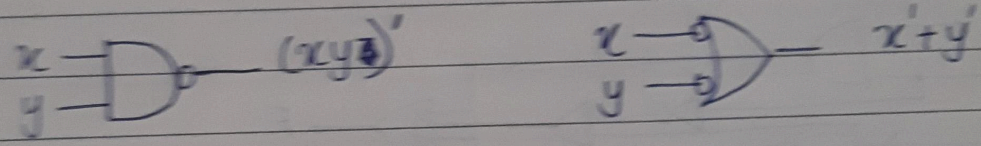
proves $(x+y)' = x'y'$ ⇒ NOR gate

$(xy)' = x'+y'$ ⇒ NAND gate

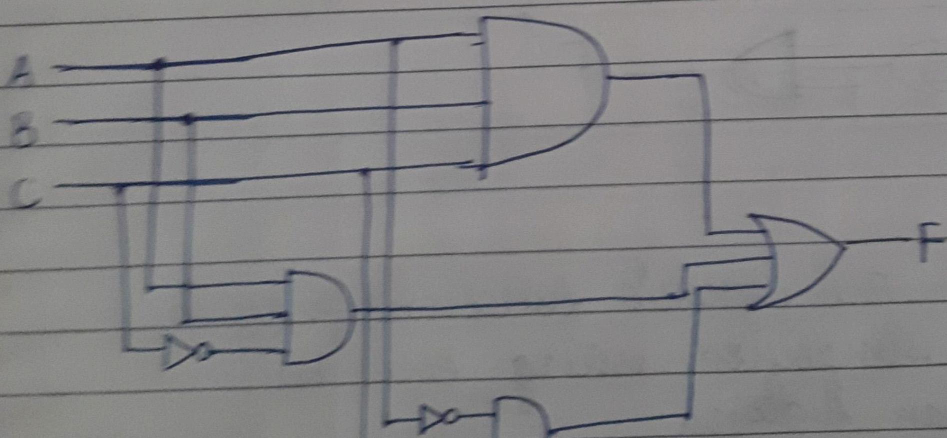
NOR Gate



NAND Gate



$F = ABC + ABC' + A'C$

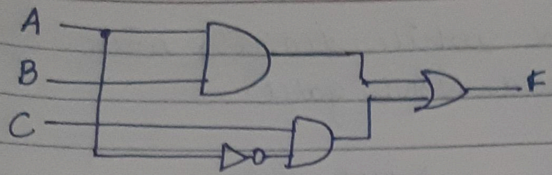


F can be represented as

$F = AB(C+C') + A'C$

$= AB + A'C$

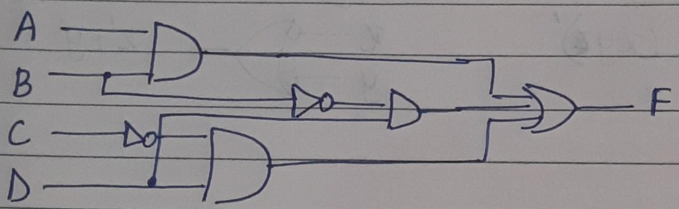
X

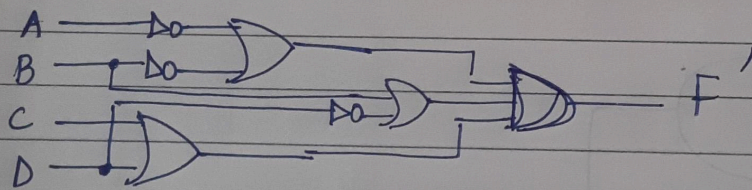


Complement of a Function

When $F = AB + C'D + B'D$

$F' =$ ~~$(A+B)'$~~ $(A'+B')(C+D)(B+D')$.





<u>Map Simplification</u>. The algebric functions may be simplified using the basic relations of Boolean Algebra.

The map-method is regarded as a pictorial arrangement of the truth table.

This method is also known as the <u>K-map</u> or ~~Knau~~ <u>Karnaugh map</u>.

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Combinational Circuits

A combinational circuit is a connected arrangement of logic gates with a set of inputs and outputs.

Block diagram.

n input variables → combinational circuits → m output variables.

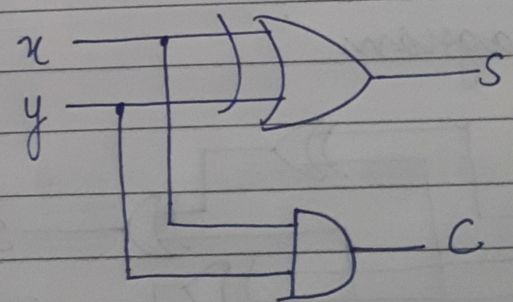
Combinational circuit can be described by a truth table showing the binary relationship b/w the n input variables and the m output variables.

Half Adder A combinational circuit that performs the arithmetic addition of 2 bits.

Truth table:

x	y	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

logic diagram:



boolean functions:

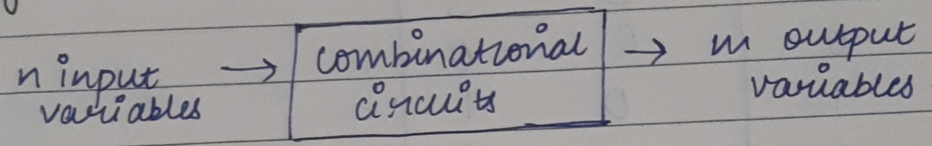
$S = x'y + xy' = x \oplus y$ — XOR gate.

$C = xy$ — AND gate

Combinational circuits

A combinational circuit is a connected arrangement of logic gates with a set of inputs and outputs.

Block diagram.



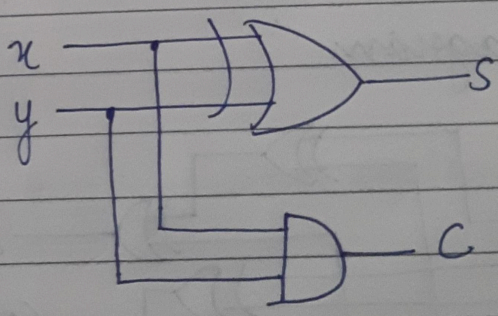
combinational circuit can be described by a truth table showing the binary relationship b/w the n input variables and the m output variables.

Half Adder A combinational circuit that performs the arithmetic addition of 2 bits.

Truth table:

x	y	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

logic diagram:



boolean functions:

$S = x'y + xy' = x \oplus y$ — ~~NAND~~ XOR gate.

$C = xy$. — AND gate

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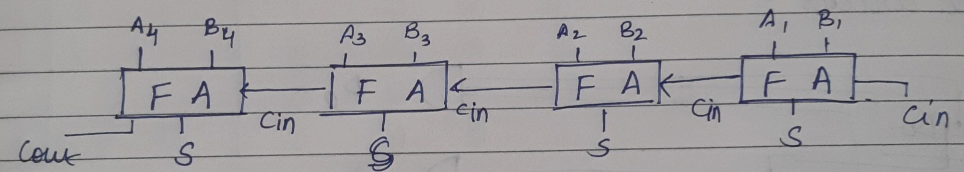
Parallel Adder It is a combination of various full adder.

A 4 bit 11 adder has 4 full adders

ex.

	A_1	A_2	A_3	A_4
	1	1	0	1
+	1_{B_1}	1_{B_2}	1_{B_3}	0_{B_4}
1	1	0	1	1



Decoder It is a combinational circuit that converts binary digits into equivalent decimal numbers.

It converts n binary digits into equivalent decimal codes.

They have n inputs and 2^n outputs.

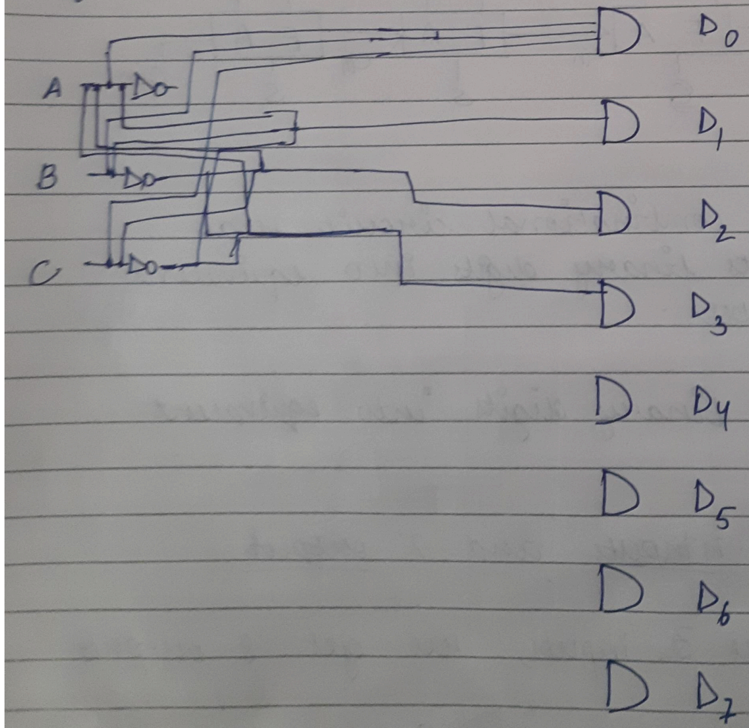
If we have 3 inputs, we get 8 outputs

Such a decoder is known as 3 to 8 line decoder

Truth table:

A	B	C	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	1	0	0	0	0	0	0	1	0	0
0	1	1	0	0	0	0	1	0	0	0
1	0	0	0	0	0	1	0	0	0	0
1	0	1	0	0	1	0	0	0	0	0
1	1	0	0	1	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0

logic circuit :



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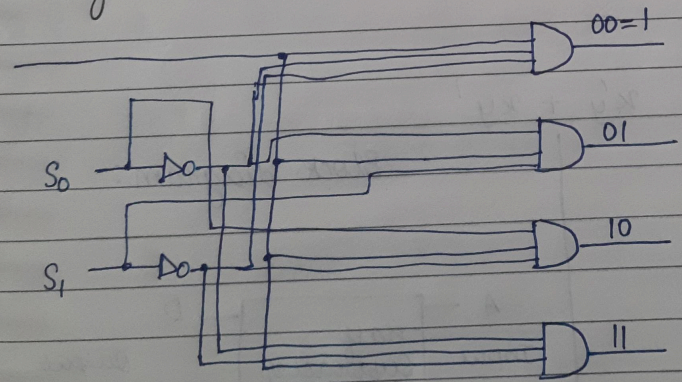
<u>De-Multiplexer</u> It is a combinational circuit in which input is divided into 1 to 2^n output. where n is the number of selection lines.

If there are 2 to selection lines, ie. $n=2$, there will be 4 outputs.

Such a de-multiplexer (De-mux) is known as 1 to 4 de mux

E	S_0	S_1	D_0	D_1	D_2	D_3
1	0	0	1	0	0	0
1	0	1	0	1	0	0
1	1	0	0	0	1	0
1	1	1	0	0	0	1

Logic circuit



$0 = a'$ $1 = a$

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Half Subtracter

1	0	1	0
− 1	− 0	− 0	− 1
0 0	0 0	0 1	1 1
B D	B D	B D	B D

X	Y	D	B
0	0	0	0
0	1	1	1 ✓
1	0	1	0
1	1	0	0

D → XOR Gate

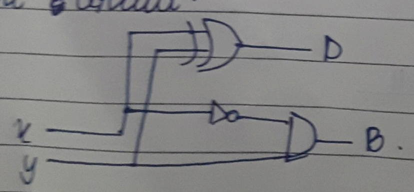
$x'y$

Logic eq^n $x' = 0$ $x = 1$

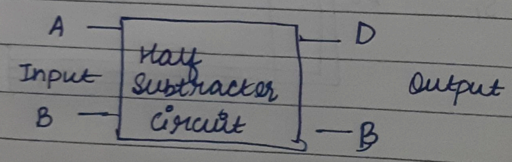
D : $x \oplus y = x'y + xy'$

B : $x'y$

Logic circuit:



Block diagram:



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Full Subtracter

```
  1 1 0 0
- 1 0 1 1
  0 0 0 1
```

```
  1 1 0 1 0
- 1 0 1 0 1
  0 0 1 0 1
```

~~logic~~ Truth Table

	Input			Output	
	A	B	Borrow$_{in}$	Diff	Borrow
	0	0	0	0	0
$x'y'$	0	0	1	1	1
$x'y$	0	1	0	1	1
$x'y$	0	1	1	0	1
	1	0	0	1	0
	1	0	1	0	0
	1	1	0	0	0
xy	1	1	1	1	1

logic eq^n

$D = A \oplus B \oplus B_{in}$

$B_{out} = A'B'C + A'BC' + A'BC + ABC$

$= A'(B'C + BC') + (A'+A)BC$

$= A'(B \oplus C) + BC$