Bittoo TRADE MARK REGD.

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Combinational	Sequential
Output of cc is entirely dependent on its inputs	Output of sc also depends on the clock pulse as well as the storage elements.
They are ready to use, and there is no need to control them	They are controlled by the clock ~~pt~~ pulse
ex: full adder, half adder, decoder, encoder, mux, de-mux	ex: flip-flop, registers, counters.

Sequential circuits - are combination of logic gates, clock pulse and storage elements -

Flip Flop. The storage elements ~~employed~~ required in by sequential ~~sem~~ circuits are called flip flops.
It has 2 states on and off.
They are bistable devices that store 1 bit of information at a time. (0 or 1)
They have some inputs, a clock pulse and an output.
Commonly used flip flops:
① SR ② JK ③ D ④ T ⑤ Master - slave

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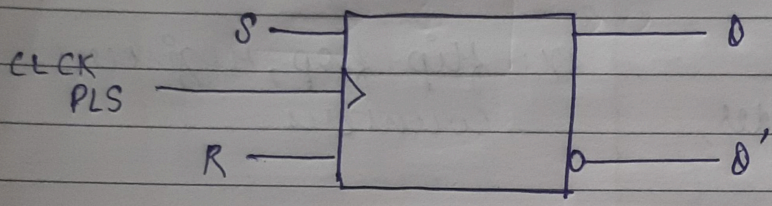
① SR flip flop

It has 2 inputs S (set) and R (reset) and 2 outputs Q and Q'.

S is for 1 and R is for 0.

Block diagram for SR flip flop is



Working of SR flip flop can be explained with the help of its truth table.

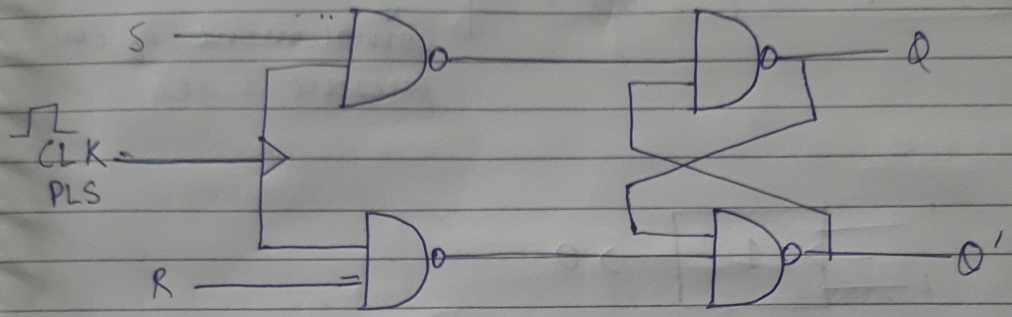
S	R	Q next
0	0	no change
0	1	reset (0)
1	0	set (1)
1	1	? Indeterminate

This drawback is called Race condition

When both inputs S and R are high (1) then, this flip flop does not give a certain output. This is called indeterminate state. It happens because both inputs are high and there is a race between them. Hence, it is called race condition

This problem is solved by JK Flip Flop.

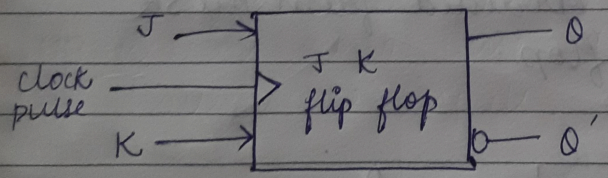
Logic circuit



(2) JK Flip Flop.
Invented (rectified) by Jack Kirby

It has 2 inputs J and K and
2 outputs as well.

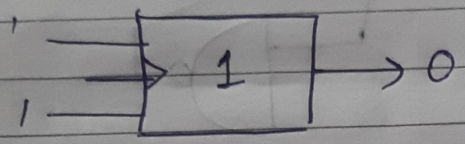
Block diagram for JK flip flop is:

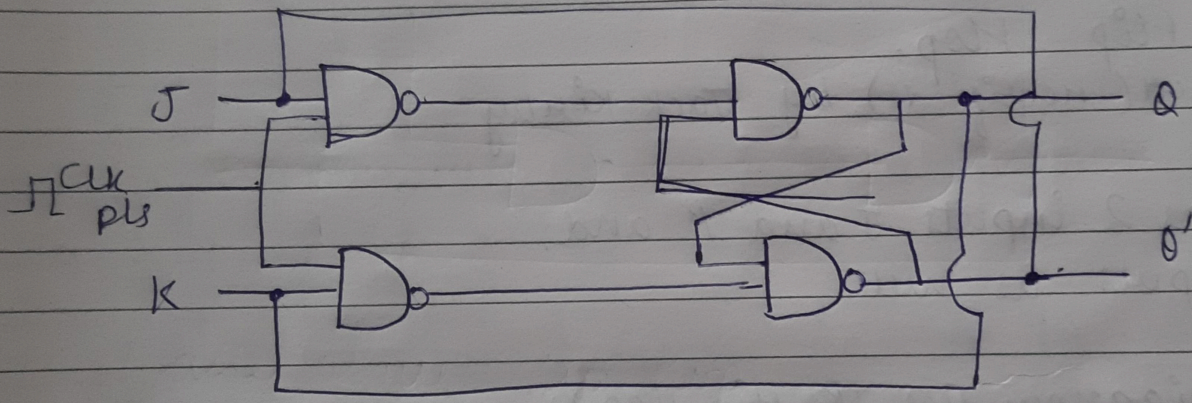


The working of JK flip flop can be explained with the help of its truth table.

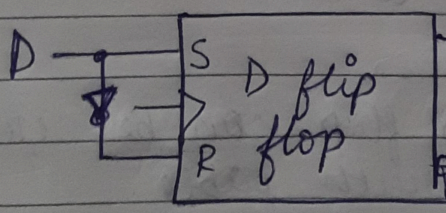
J	K	Output
0	0	no change
0	1	reset (0)
1	0	set (1)
1	1	Q'(t)

↓ complement of the present state





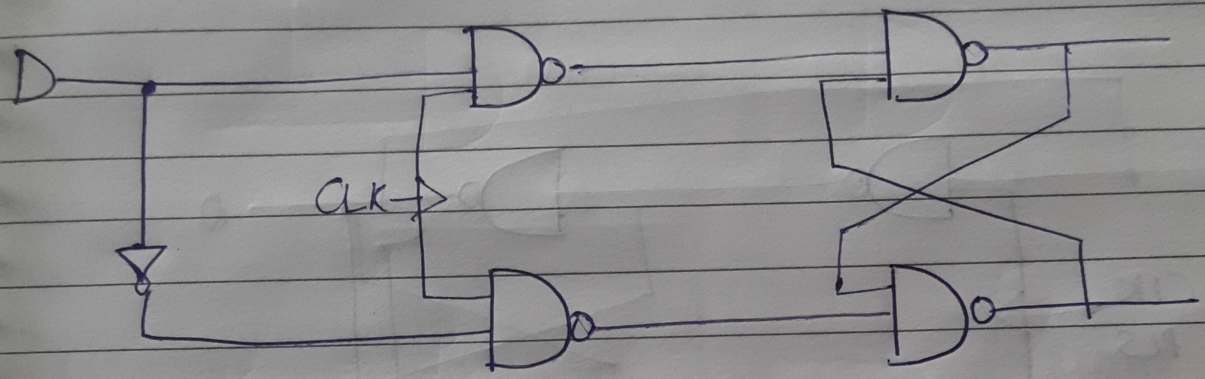
③ D flip flop It is obtained from the SR flip flop.



The D flip flop can be obtained by combining S and R inputs into a single input with the help of NOT Gate

It has 1 input named D so there will only be 2 combinations in the truth table

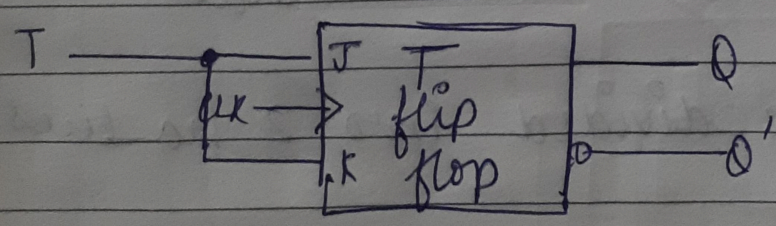
D	Output
0	Reset (0)
1	Set (1)



This cross conn" is called LATCH

④ T flip flop It is obtained from JK flip flop

Can be obtained by combining the J and K inputs into one input

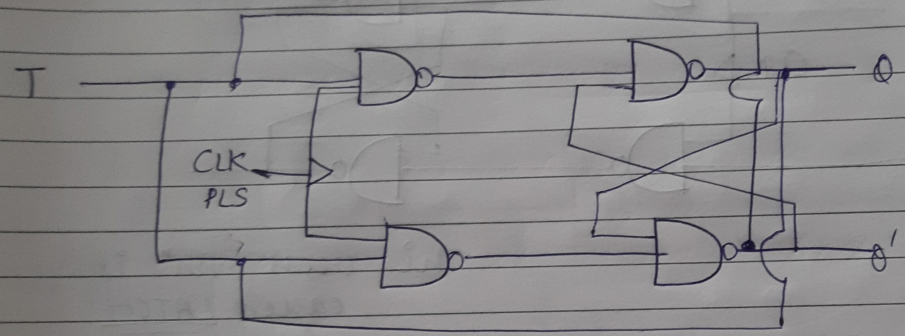


Truth Table

T	Qnext
0	no change
1	Q'(t)

↳ complement of present state

T → Toggle

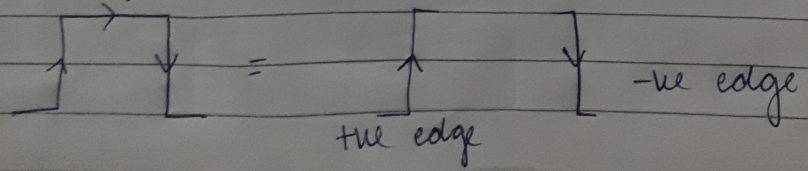


(5) Master Slave flip flop

It is a combination of 2 flip flops

Master Slave.

Here, one clock pulse is divided into 2 halves
first half → +ve edge
second half → -ve edge



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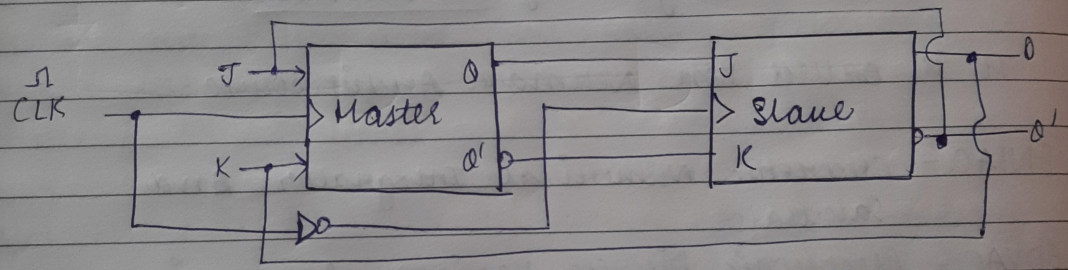
The +ve edge goes from low to high.
The -ve edge goes from high to low.

Master will change its state on occurence of +ve pulse / edge.

Slave will change its state on the occurance of -ve pulse / edge.

Block Diagram



logic circuit