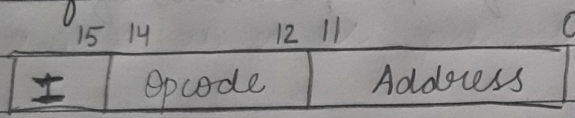
Types of Instructions

- MRI (Memory Reference Instr")
  - Direct MRI
  - Indirect MRI
- Non MRI
  - Register Reference Instr"
  - I/O reference Instr"

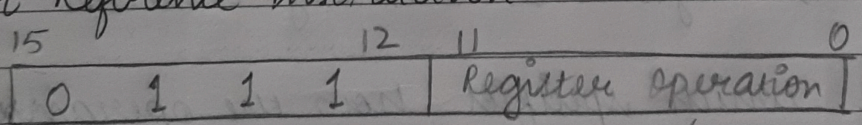
① Memory Reference Instruction



(Opcode = 000 through 110)

In memory reference instruction, 12 bits of memory is used to specify an address and one bit to specify the addressing mode 'I'

② Register Reference Instruction



(opcode = 111, I = 0)

The register reference instructions are represented by the opcode 111 with 0 in the leftmost bit (bit 15) of the instruction.

A register reference instruction specifies an operation on or a test of the AC register.

③ Input Output instruction

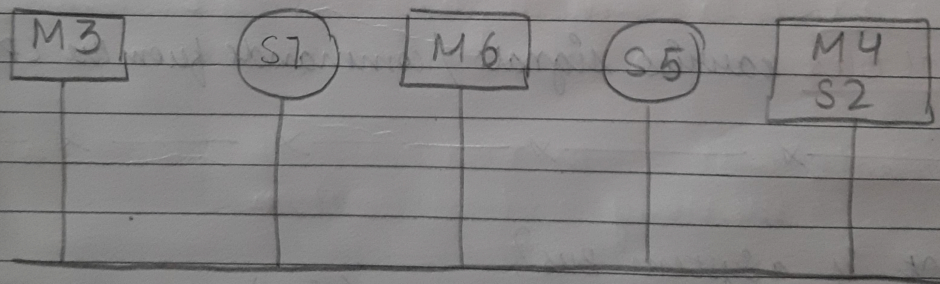
15	14	13	12	11 ... 0
1	1	1	1	I/O operation

(opcode = 111, I = 1)

The input output instr^{n} does not need a reference to memory and is recognized by the operation code 111 with a 1 in the leftmost bit of the instruction.
The remaining 12 bits are used to specify the type of the input-output operation or test performed.

COMMON BUS SYSTEM

A pair of signal lines that facilitate the transfer of multi-bit data from one system to another is known as a bus.



Here M3, M6 and M4 are the three Master devices. These are the ones that ~~control~~ start and control the connection.
S7, S5 and S2 are the slave devices that counter to the commands provided by master devices.

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When a master device needs to offer a command to a slave device, it should transfer its instruction by a bus.

The basic comp includes 8 registers, a memory unit, and a control unit. These units require to connect frequently. A bus supports the medium through which comm" can take ~~place~~ place.

Types of Busses

(1) Address Bus carries the address of data (but not the data) between the processor and the memory.

(2) Data Bus carries the data between the processor, the memory unit and the input/output devices

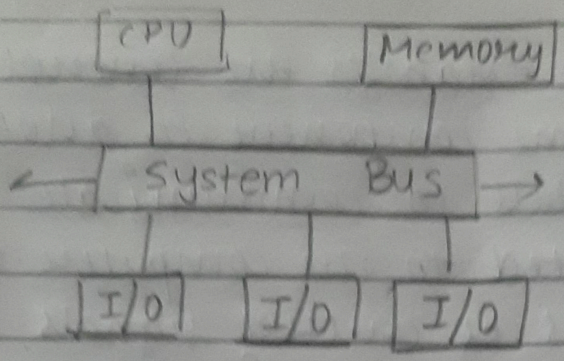
(3) Control Bus carries signals / commands from the CPU

Ques what is a System Bus?

A bus is a set of electrical wires (lines) that connects the various hardware components of a computer system.

It works as comm" pathway through which info. flows from one hardware component to another.

A bus that connects major components (CPU, memory, I/O devices) of a comp system is called a System Bus



Why do we need Bus?

- A comp syst is made of different components such as memory, ALU, etc.
- Each comp should be able to communicate with the other for the proper execution of instructions and instruction flow.
- Implementing a mesh topology among different components would be really expensive.
  So we use a common component to connect each necessary component, ie; Bus.

Components of System Bus

- Data Bus
- Address Bus
- Control Bus

Data Bus is used for transmitting the data and instructions from the CPU to memory, I/O and vice-versa. It is bi-directional.

Address Bus is used to carry address from CPU to memory I/O devices. It is used to identify the particular location in the memory. It carries the source or destination address of data (where to store or from where to retrieve the data).
It is uni-directional.

Control Bus is used to transfer the control and timing signals from one component to another. The CPU uses the control bus to communicate with the devices that are connected to the computer system. CPU transmits different types of control signals to the system components. It is bi-directional.

Q What are control and timing signals?

- Control signals are generated in the control unit of the CPU.

- Timing signals are used to synchronize the memory and I/O operations with a CPU clock.

Typical control signals held by the Control Bus:

Memory Read — Data from memory address location to be placed on data bus.

Memory Write — Data from data bus to be placed on memory address location.

I/O Read — Data from I/O address location to be placed on data bus

I/O Write — Data from data bus to be placed on I/O address location

Other control signals held by control bus: interrupt,

interrupt acknowledge, bus request, bus ~~grand~~ grant and several others.
The type of action taking place on the system bus is indicated by these control signals.

Data Movement among registers using Bus

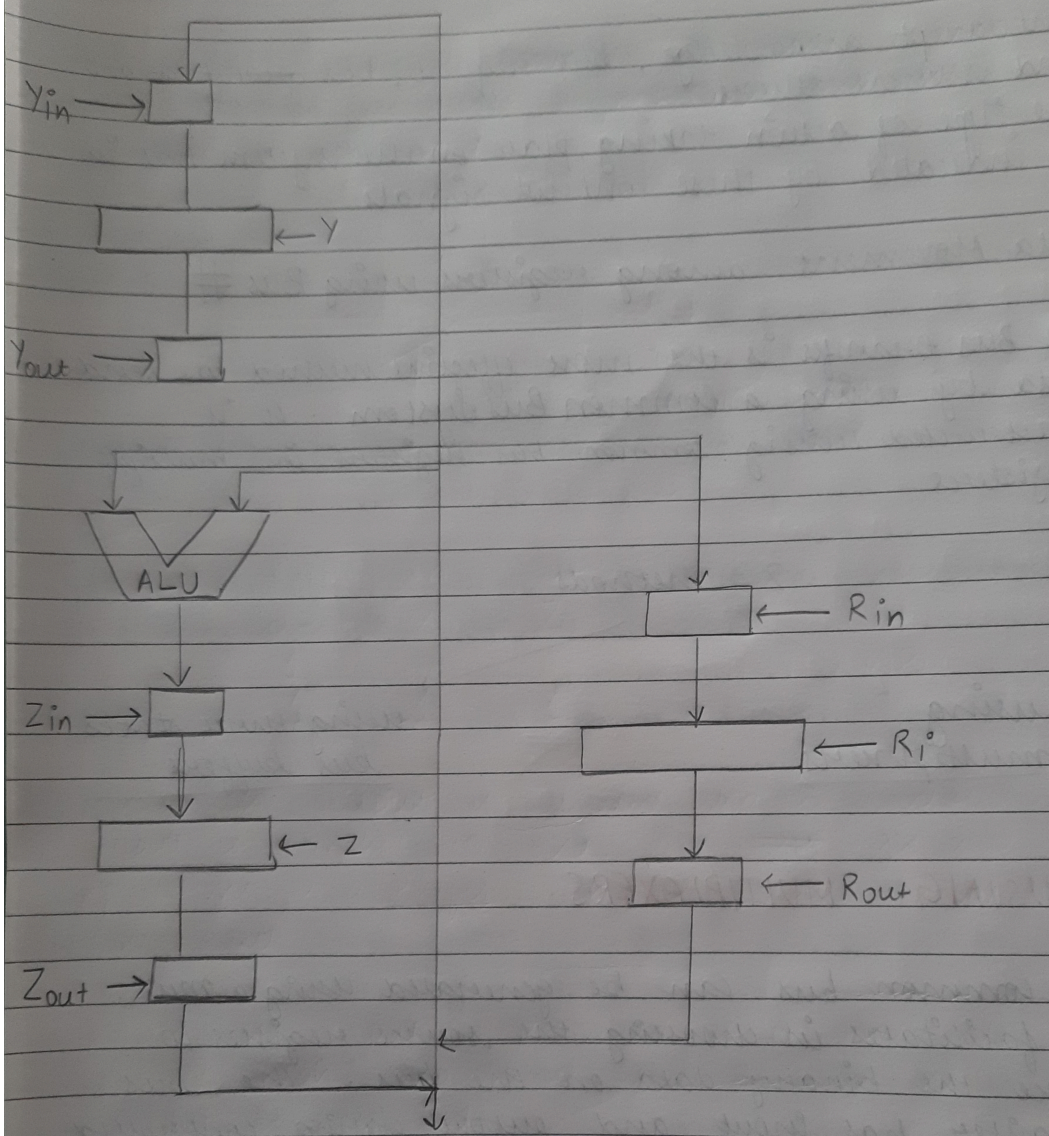
The Bus transfer is the most effective method to send data by using a Common Bus System. It is constructed using common bus registers in multiple registers

2 methods

- using multiplexers
- using three states bus buffers

(1) USING MULTIPLEXERS.

A common bus can be generated using a mux. It facilitates in choosing the source register to place the binary data on the bus. The bus register has input and output gating controlled by control signals.



* R_i is the register ; R_{in} and R_{out} are the input and output gating ~~signals~~ of R_i signals
* Z is the register ; Z_{in} and Z_{out} are the input and output gating ~~signals~~ signals of Z
* Y is the register ; Y_{in} and Y_{out} are the input and output gating signals for Y

The switches are controlled by the control signal.

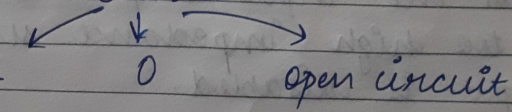
When the signal is ON, R_i is set to 1
" " " " OFF, R_i is set to 0.

When the input gating R_{in} is set to 1, the data is loaded into the register bus R_i accessible to the common bus.
When R_{out} is set to 1, contents of the register R_i are placed on the data bus.
It is reffered to as input enabled and output enabled signals.
The functs that take place inside the processor are in sync with the clock pulse

(2) THREE STATE BUFFERS.

Three state buffers can generate a common bus. Buffer is an area of the memory, which is added in b/w devices to block several interactions and to connect their support.

Buffer is established on 3 states



- The logic 0 and 1 are the two signals similar to the ones in the conventional gate
- The three-state gates can ~~be~~ implemented any ~~to~~ conventional logic – AND or NAND, OR or NOR

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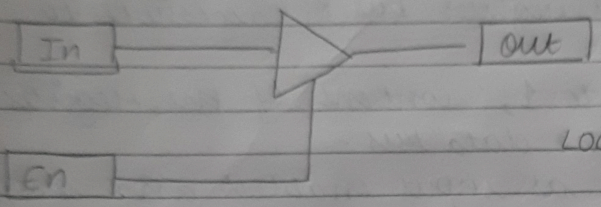
- The high impedance state defines that it does not contain the logic significance and the output is seperated



LOGIC SYMBOL

En	In	Out
0	X	Z
1	0	0
1	1	1

TRUTH TABLE

- When the output is allowed and the control input is similar to one. The ~~logig~~ logic gate performs as a Buffer with the output similar to the input.

- When the input is provided is 0, the gate goes too high impedance state Z and the output is disabled.

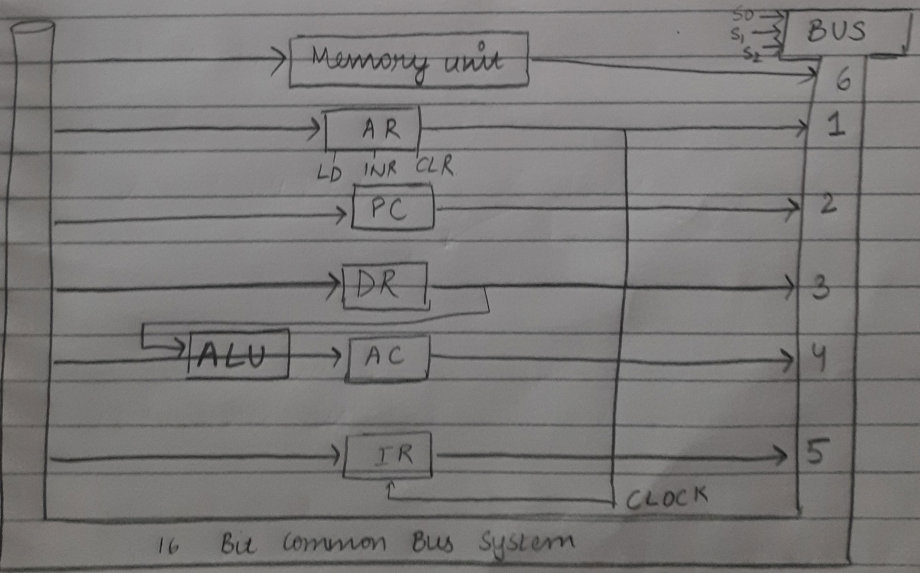
- The impedance in three-state buffers linked all the outputs with a cable to produce a common bus line and does not threaten the loading effect.

- The truth table shows that when some input is given and gate is disabled, it shows in high impedance.
- When the gate is enabled, with some input given, then the output results are not in disabled mode.
- When the gate is enabled with input as 1, the output is similar to 1.

Common Bus System

A pair of signal that facilitates the transfer of multi-bit data from one system to another is known as BUS.

A basic computer has 8 registers, a memory unit, and a control unit.



16 Bit Common Bus System

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List of registers are:

① AR Address register It holds the address of the operand
length is 12 bits.

② Program Counter It contains the address of the next instruction to be executed
length is 12 bits.

③ Data Register It contains the operand
length is 16 bits

④ Accumulator It performs all the calculations and is also known as Processor Register